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(54)【発明の名称】　半導体電子部品の製造方法およびウエハ

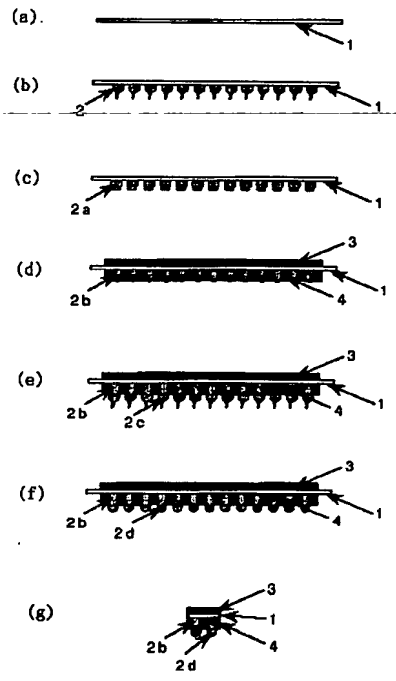
(57)【要約】

【課題】半導体電子部品をそのチップサイズとほぼ同程度の大きさにて、しかも高信頼のものを安価に製造，提供する事を目的とする。

【解決手段】ウエハを基本単位としてＰＫＧ工程を経る。

【効果】最も安価で信頼性の高いチップサイズＰＫＧが得られる。

図１



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Search scope: US EP WO JP; Full patent spec.
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JP09219421
MANUFACTURE OF SEMICONDUCTOR ELECTRONIC COMPONENT AND WAFER
HITACHI LTD
Inventor(s): HASEBE AKIO ; MIYAMOTO TOSHIO ; ARIMA HIDEO ; YAMAMOTO KENICHI ; HARUTA AKIRA ; TSUBOSAKI KUNIHIRO ; MORINAGA KENICHIRO
Application No. 08026434, Filed 19960214, Published 19970819

Abstract: PROBLEM TO BE SOLVED: To shorten a TAT and reduce the cost of the TAT by a method wherein stud bump electrodes made of solder are respectively formed again on the point parts of first-layer electrodes, second-layer electrodes of a shape uniformized by reflowing the stud bump electrodes are formed and a wafer is diced into chips to obtain chip-sized packages.

SOLUTION: Solder stud bump electrodes 2 formed on a wafer 1 are subjected to leveling, electrodes 2a are formed and organic materials 3 and 4 are respectively provided on both surfaces of the surface and rear of the wafer 1 formed with the electrodes 2a making to interpose the wafer 1 between them by molding, coating or the like. A surface treatment, such as a polishing treatment, of these bump electrodes 2a and first electrodes 2b is performed, which respectively have a bump electrode upper part which is new and is easily wetted, are formed. Solder stud bump electrodes 2c are respectively formed again on the point parts of the electrodes 2b, the wafer 1 is reflowed to form second electrodes 2d obtainable by making even the electrodes 2c and the wafer 1 is diced into chips to obtain chip-sized packages.

Int'l Class: H01L02160; H01L021301 H01L021321

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